

**IN THE ABSTRACT OF THE DISCLOSURE:**

Please amend replace the abstract as follow with the following new abstract:

**ABSTRACT**

A semiconductor integrated circuit has ~~over one semiconductor substrate a~~ nonvolatile memory and a logic circuit which uses information stored in the nonvolatile memory to perform logical operation. The nonvolatile memory comprises bit lines ~~(bl and blb)~~, word lines ~~(wl<sub>n</sub>)~~, and memory cells ~~(20)~~. The memory cell comprises MOS transistors ~~(M1 and M2)~~ whose gate electrodes are connected with a word line. Information storage is carried out according to whether one source/drain electrode of the MOS transistors is connected with a source line ~~(cs)~~ or floated. During ~~the~~ other periods than a predetermined period in the operation of accessing the memory cell, the potential difference between the source/drain electrodes of the MOS transistors constituting the memory cell is zeroed. ~~Therefore,~~ subthreshold Subthreshold leakage current is prevented from ~~being passed~~ passing through the memory cell on standby. During the predetermined period in accessing operation, a potential difference is produced between the source/drain electrodes of the MOS transistors. Therefore, the bit line potential can be varied by word line selection.